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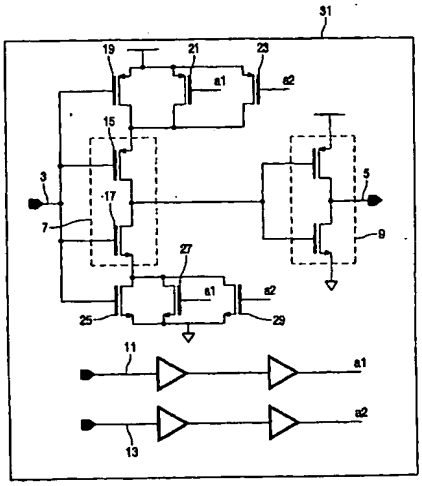
(54) Title: BUFFER CIRCUIT



(57) Abstract: A buffer circuit (31), for example a repeater or receiver circuit for a signal wire of an on-chip bus, receives an input signal, and produces an output signal. The buffer circuit (31) comprises a first inverting stage (7) and a second inverter stage (9). The second inverting stage (9) provides the drive for the output (5). The first inverting stage (7) has additional circuitry (15, 17, 19, 21, 23, 25, 27, 29) for controlling the strengths of the pull up path and the pull down path. The pull up/down paths are dynamically controlled according to the status of one or more aggressor signals. In one embodiment the switching threshold is lowered only in the worst case delay scenario, i.e. when the signal wire (3) is at a different logic level to the aggressor signals. In another embodiment, the switching threshold is raised when the signal wire and aggressor signals are all at the same logic level, thereby reducing crosstalk.

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